INDIAN INSTITUTE OF TECHNOLOGY PATNA

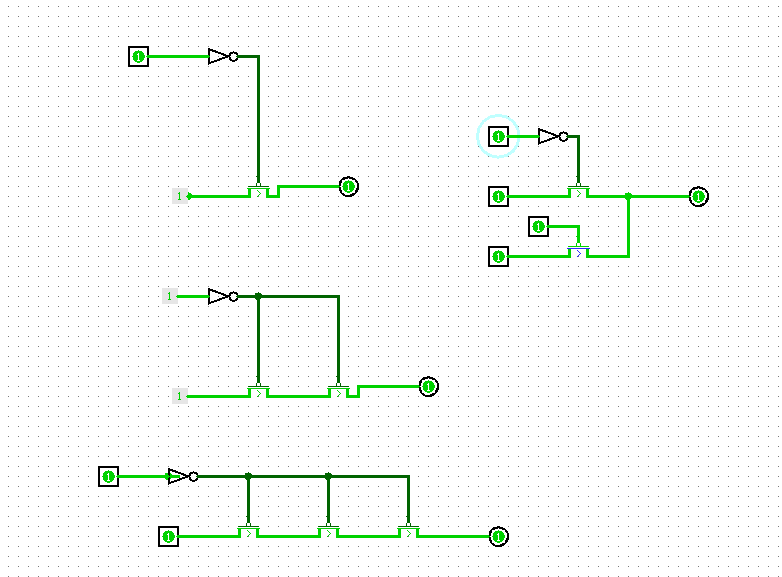
CS226- Switching Theory Lab

**Lab 2: Logic simulation Sub-blocks**

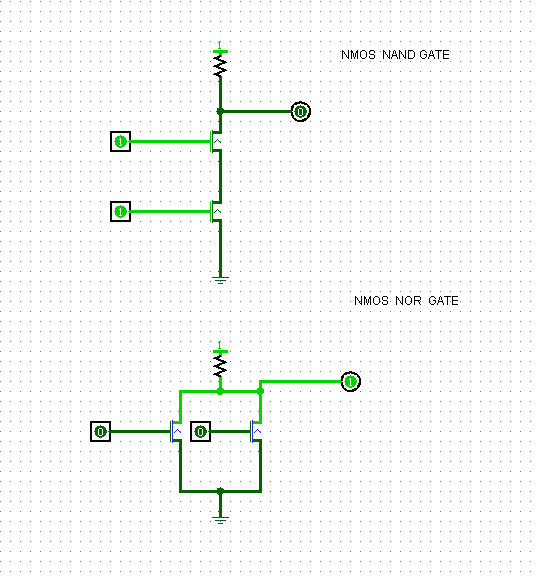
Exercise 1 (series parallel structures):

Simulate the following structures:

(Follow Lab1 steps to simulate)



Exercise 2 (NMOS gates):

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**Assignment:**

(Design and simulate)

1. Create series structure with 4 PMOS/NMOS transistors and verify the functionality ( Assume A, B,C, and D are the inputs). **(5 points)**

1. Using NMOS logic, create 5 input NAND, NOR, AND and OR gates. **(10 points)**
2. Implement the following using CMOS Logic.

**Y=  (10 points)**

1. Implement the following using CMOS Logic.

**Y=  (5 points)**

1. Create a library of gates (NAN,NOR, AND, OR, XOR) from the Lab 1 and implement the following using your library( See tutorial sub-circuits). **Y=  (15points)**

1. Implement and verify the functionality using existing library of Gates in logic-sim

**Y=  (5points)**

**Submission:**

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Submit Report with hand drawn schematic is required for the problems (by end of the class). Show the simulations to TAs. Submit your .circ file containing your various transistor-level/logic level implementations

* The simulation files p1.circ, p2.circ, p3.circ, p4.circ, p5.circ and p6.circ
* Zip the above five files. Zip file name is your role number.

Course work submission through Email: [cs225.iitp@gmail.com](mailto:cs225.iitp@gmail.com)

(use email subject Lab2\_Logicsim\_your roll number).

This work is due on: : 13th January